IN THE CLAIMS:

Please amend claims 1, 2, 11, 12, 20, 21, and 30-39, as set forth below.

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1. (Currently Amended) A method comprising:

initializing a circuit said circuit having at least one memory element coupled to a memory bus on a host system;

monitoring signals on the memory bus;

detecting a first sequence of signals, the first sequence of signals including a reserved memory address, the reserved memory address comprising a particular memory address reserved for switching control of the at least one memory element; and

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switching control of the at least one memory element to the circuit in response to detection of the reserved memory address.

2. (Currently Amended) The method of claim 1 further comprising:

detecting a second sequence of signals, the second sequence of signals including another reserved memory address, the another reserved memory address comprising a second particular memory address reserved for switching control of the at least one memory element; and

switching control of the at least one memory element to the host system in response to detection of the another reserved memory address.

3. (Original) The method of claim 2 wherein error correcting codes are switched off prior to switching control of the at least one memory element to the host system.

4. (Original) The method of claim 1 wherein initializing a circuit having at least one memory element coupled to a memory bus on a host system comprises detecting a sequence of writes to memory locations on the circuit.

5. (Original) The method of claim 4 wherein the sequence of writes are writes to random memory locations on the circuit.

6. (Original) The method of claim 1 wherein monitoring signals on the memory bus comprises the circuit monitoring control, address, and data signals on the host system.

7. (Previously Presented) The method of claim 1 wherein detecting a first sequence of signals comprises detecting at least one write signal to the reserved memory address.

8. (Previously Presented) The method of claim 1 wherein detecting a first sequence of signals comprises detecting at least one read signal from the reserved memory address.

9. (Previously Presented) The method of claim 1 wherein switching control of the memory bus to the circuit comprises a processing element in the circuit reading from or writing to the at least one memory element in the circuit.

10. (Original) The method of claim 2 wherein switching control of the at least one memory element to the host system comprises a processor on the host system reading from or writing to the at least one memory element.

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11. (Currently Amended) An apparatus comprising:

a memory bus on a host system;

a plurality of memory elements on a circuit, said plurality of memory elements communicatively coupled with the memory bus;

a processing element on the circuit communicatively coupled with the plurality of memory elements and the memory bus, said processing element to

monitor signals on the memory bus;

detect a first sequence of signals, the first sequence of signals including a reserved memory address, the reserved memory address comprising a particular memory address reserved for switching control of the plurality of memory elements; and

switch control of the plurality of memory elements to the circuit in response to detection of the reserved memory address.

12. (Currently Amended) The apparatus of claim 11 further comprising said processing element to detect a second sequence of signals, the second sequence of signals including another reserved memory address, the another reserved memory address comprising a second particular memory address reserved for switching control of the plurality of memory elements; and
switch control of the plurality of memory elements to the host system in response to detection of the another reserved memory address.

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13. (Original) The apparatus of claim 12 wherein error correcting codes are switched off prior to switching control of the plurality of memory element to the host system.

14. (Original) The apparatus of claim 11 wherein the processing element is at least one of a field programmable gate array, and a processor.

15. (Original) The apparatus of claim 11 wherein the processing element to monitor signals on the memory bus comprises the processing element to monitor control, address, and data signals on the host system.

16. (Previously Presented) The apparatus of claim 11 wherein the processing element to detect a first sequence of signals comprises the processing element to detect at least one write signal to the reserved memory address.

17. (Previously Presented) The apparatus of claim 11 wherein the processing element to detect a first sequence of signals comprises the processing element to detect at least one read signal to the reserved memory address.

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18. (Original) The apparatus of claim 11 wherein the processing element to switch control of the plurality of memory element to the circuit comprises the processing element reading from or writing to the plurality of memory elements.

19. (Original) The apparatus of claim 12 wherein the processing element to switch control of the plurality of memory elements to the circuit comprises a processor on the host system reading from or writing to the plurality of memory elements.

20. (Currently Amended) An article of manufacture comprising:

a machine-accessible medium including instructions that, when executed by a machine, causes the machine to perform operations comprising

initializing a circuit said circuit having at least one memory element coupled to a memory bus on a host system;

monitoring signals on the memory bus;

detecting a first sequence of signals, the first sequence of signals including a reserved memory address, the reserved memory address comprising a particular memory address reserved for switching control of the at least one memory element; and

switching control of the at least one memory element to the circuit in response to detection of the reserved memory address.

21. (Currently Amended) The article of manufacture as in claim 20, further comprising instructions for detecting a second sequence of signals, the second sequence of signals including another reserved memory address, the another reserved memory address comprising a second particular memory address reserved for switching control of the at least one memory element; and

switching control of the at least one memory element to the host system in response to detection of the another reserved memory address.

22. (Original) The article of manufacture as in claim 21, further comprising instructions for switching of error correcting codes prior to switching control of the at least one memory element to the host system.

23. (Original) The article of manufacture as in claim 20, wherein said instructions for initializing a circuit having at least one memory element coupled to a memory bus on a host system comprises further instructions for detecting a sequence of writes to memory locations on the circuit.

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24. (Original) The article of manufacture as in claim 23, wherein said instructions for detecting a sequence of writes include further instructions for writing to random memory locations on a circuit.

25. (Original) The article of manufacture as in claim 20, wherein said instructions for monitoring signals on the memory bus comprises further instructions for the circuit monitoring control, address, and data signals on the host system.

26. (Previously Presented) The article of manufacture as in claim 20, wherein said instructions for detecting a first sequence of signals comprises further instructions for detecting at least one write signal to the reserved memory address.

27. (Previously Presented) The article of manufacture as in claim 20, wherein said instructions for detecting a first sequence of signals comprises further instructions for detecting at least one read signal from the reserved memory address.

28. (Previously Presented) The article of manufacture as in claim 20, wherein said instructions for switching control of the memory bus to the circuit comprises further instructions for a processing element in the circuit reading from or writing to the at least one memory element in the circuit.

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29. (Original) The article of manufacture as in claim 21, wherein said instructions for switching control of the at least one memory element to the host system comprises further instructions for a processor on the host system reading from or writing to the at least one memory element

30. (Currently Amended) The method of claim 1, wherein the ~~reserved~~ particular memory address ~~corresponds to a reserved~~ comprises an address in the at least one memory element in the circuit.

31. (Currently Amended) The method of claim 1, wherein the ~~reserved~~ particular memory address ~~corresponds to a reserved~~ comprises an address in a second memory coupled with the memory bus.

32. (Currently Amended) The apparatus of claim 11, wherein the ~~reserved~~ particular memory address ~~corresponds to a reserved~~ comprises an address in the plurality of memory elements of the circuit.

33. (Currently Amended) The apparatus of claim 11, wherein the ~~reserved~~ particular memory address ~~corresponds to a reserved~~ comprises an address in a second memory coupled with the memory bus.

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34. (Currently Amended) The article of manufacture of claim 20, wherein the ~~reserved~~ particular memory address ~~corresponds to a reserved~~ comprises an address in the at least one memory element in the circuit.

35. (Currently Amended) The article of manufacture of claim 20, wherein the ~~reserved~~ particular memory address ~~corresponds to a reserved~~ comprises an address in a second memory coupled with the memory bus.

36. (Currently Amended) A method comprising:

monitoring signals on a memory bus, the memory bus coupled with a memory and a first processor; and

in response to detecting a reserved memory address on the memory bus, switching control of the memory from the first processor to a second processor coupled with the memory bus, wherein the reserved memory address comprises a particular memory address reserved for switching control of the memory.

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37. (Currently Amended) The method of claim 36, further comprising:

in response to detecting another reserved memory address on the memory bus, switching control of the memory from the second processor to the first processor, wherein the another reserved memory address comprises a second particular memory address reserved for switching control of the memory.

38. (Currently Amended) The method of claim 36, wherein the ~~reserved~~ particular memory address ~~corresponds to a reserved~~ comprises an address in the memory.

39. (Currently Amended) The method of claim 36, wherein the ~~reserved~~ particular memory address ~~corresponds to a reserved~~ comprises an address in a second memory coupled with the memory bus.

40. (Previously Presented) The method of claim 36, wherein detecting the reserved memory address comprises detecting one of a read to the reserved memory address and a write to the reserved memory address.

41. (Previously Presented) The method of claim 36, wherein the memory and the second processor comprise part of a single component.

42. (Previously Presented) The method of claim 41, wherein the single component comprises a dual inline memory module (DIMM) coupled with the memory bus.

43. (Previously Presented) The method of claim 36, wherein the memory comprises a synchronous dynamic random access memory (SDRAM).